Low power methodology manual for system-on-chip design

A Model Driven Engineering (MDE) approach to automate low power design intent specifications and accelerate Low Power Design Intent Space Exploration (LPDISE) using a Transaction-Level power-aware design methodology that mainly relies on a high level

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Low Power Methodology Manual: For System-on-Chip Design. July 2007. Authors: Michael Keating, David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi. Publisher: Springer Publishing Company, Incorporated, ISBN: 0387718184. Published: 31 July 2007. Pages: 304. Get Citation Alerts. Save to Binder. Export Citation. 0. Abstract.

This book provides a practical guide for engineers doing low power System-on-Chip (SoC) designs. It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches.

Abstract. Tools alone aren"t enough to reduce dynamic and leakage power in complex chip designs - a well-planned methodology is needed. Following in the footsteps of the successful Reuse Methodology Manual (RMM), authors from ARM and Synopsys have written this Low Power Methodology Manual (LPMM) to describe [such] [a] low-power methodology with ...